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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,177	04/22/2004	Hiroshi Takeda	Q81128	6047

23373   7590   10/12/2007
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EXAMINER
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ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
10/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 August 2007</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,11-13,15-17,19,20 and 25-27* is/are rejected.

7)☒ Claim(s) *4,7-10,14,18 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All   b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail. Date _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed on August 22, 2007 have been fully considered but they are

not persuasive.

Applicant argues that the reference cited Morita (USPN 6750840) does not teach

supplying a write-in-voltage for a period corresponding to the distance from the row line to end

points. However, as clearly shown in the art rejection below, Morita teaches the data signal

voltage to be supplied to the individual pixels corresponding to the line that is to be scanned is

changed by the voltage transformation circuit (24). Based on the distance between the selected

pixel and the data-line drive circuit (22), a boosted, high voltage is supplied to the data line X in

a given period within the selection period (col. 12, lines 51-59, Fig. 9 (22, 24)). Applicant argues

that Morita does not teach first and second timing signal at constant intervals and generating a

third timing signal at intervals increasingly variable as a function of distance. However, as shown

in the art rejection below, Morita teaches as illustrated in FIGS. 10A to 10C and FIGS. 11A to

11C, it is possible to execute such control as to charge each pixel selected in the predetermined

period t by boosting the predetermined voltage V.sub.1 to a certain voltage level and **changing**

the period in which the boosted voltage is applied (col. 12, lines 26-30). Note that a boosted

voltage is supplied to the data line X in a given period within a selection period based on the

distance between the selected pixel and the data line drive circuit (col. 12, lines 55-57).

It would have been obvious to one of ordinary skill in the art at the time the invention

was made to recognize changeable period in which the boosted voltage is applied as illustrated in

Fig.11B (by changing a portion of a period starting from t.sub.1 but before t.sub.b3 so as to extend the constant interval beyond t.sub.1) for the purpose of improving a charge characteristics of pixels as taught by Morita (col. 12, lines 26-27, col. 11, lines 48-51).

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-3, 11-12, 15-17 and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Morita (USPN 6750840).

Regarding claim 1, Morita teaches a liquid crystal display apparatus comprising *(col. 10, lines 62-64, LCD device, see Fig. 9)*: a liquid crystal display panel comprising a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells *(col. 7, lines 20-43, Fig. 9 (10, M (m, n), Y, X, 30), pixels formed in the liquid crystal panel 10 are defined by M(1, 1) to M(m, n), where m and n are*

natural numbers, a liquid crystal panel 10 has (m.times.n) pixels (e.g.,

m=800 and n=600 in the embodiment), for one pixel M(1, 1), a data line

X.sub.1 is connected to the source of a thin film transistor (TFT) device 30

and a line Y.sub.1 is connected to the gate thereof, data lines X.sub.1 to

X.sub.m are driven by a data-line drive circuit 22 and the voltage

transformation circuit 25, while lines Y.sub.1 to Y.sub.n are driven by the

line drive circuit 20) ; and a driving circuit *(Fig. 9 (12, 20, 22, 25, 26))* for

successively generating a plurality of write-in voltages *(col. 3, lines 59-60, Fig. 9 (22),*

a data line drive circuit (22) which supplies a data signal to each of the data

lines, col. 7, lines 54-56, the signal control section 12 sends data signals

Da, a clock signal CLK1 and a horizontal sync signal Hsync to the data-line

drive circuit 22, col. 8, lines 5-6, the data signal voltage vd is output from

the data-line drive circuit 22, note that as shown in Fig. 9, data lines X.sub.1

to X.sub.m are driven by a data-line drive circuit 22), successively selecting each

of said row lines *(col. 2, lines 4-6, Fig. 9 (20), a scan-line drive circuit (20)*

which supplies a scan signal to each of the scan lines for selecting one of the

scan lines) and supplying said write-in voltages from end points of the column lines to the

liquid crystal cells of the selected row line for a period corresponding to a distance from the

selected row line to said end points *(col. 12, lines 51-59, Fig. 9 (22, 24), the data*

signal voltage to be supplied to the individual pixels corresponding to the

*line that is to be scanned is changed by the **voltage transformation***

circuit (24). Based on the distance between the selected pixel and the data-line drive circuit (22), a boosted, high voltage is supplied to the data line X in a given period within the selection period.)

Regarding claim 11, a method of driving a liquid crystal display, *(col. 10, lines 62-64, LCD device, see Fig. 9)* wherein the liquid crystal display panel comprises a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells *(col. 7, lines 20-43, Fig. 9 (10, M (m, n), Y, X, 30), pixels formed in the liquid crystal panel 10 are defined by M(1, 1) to M(m, n), where m and n are natural numbers, a liquid crystal panel 10 has (m.times.n) pixels (e.g., m=800 and n=600 in the embodiment), for one pixel M(1, 1), a data line X.sub.1 is connected to the source of a thin film transistor (TFT) device 30 and a line Y.sub.1 is connected to the gate thereof, data lines X.sub.1 to X.sub.m are driven by a data-line drive circuit 22 and the voltage transformation circuit 25, while lines Y.sub.1 to Y.sub.n are driven by the line drive circuit 20)*, the method comprising the steps of: a) generating a plurality of write-in voltages *(col. 3, lines 59-60, Fig. 9 (22), a data line drive circuit (22) which supplies a data signal to each of the data lines, col. 7, lines 54-56, the signal control section 12 sends data signals Da, a clock signal CLK1 and a*

horizontal sync signal Hsync to the data-line drive circuit 22, col. 8, lines 5-6, the data signal voltage vd is output from the data-line drive circuit 22, note that as shown in Fig. 9, data lines X.sub.1 to X.sub.m are driven by a data-line drive circuit 22) b) successively selecting one of said row lines *(col. 2, lines 4-6, Fig. 9 (20), a scan-line drive circuit (20) which supplies a scan signal to each of the scan lines for selecting one of the scan lines)*; and c) successively supplying said write-in voltages from said end points of the column lines to the liquid crystal cells of the selected row line for a write-in period corresponding to the distance from the selected row line to said end points *(col. 12, lines 51-59, Fig. 9 (22, 24), the data signal voltage to be supplied to the individual pixels corresponding to the line that is to be scanned is changed by the **voltage transformation circuit (24).** **Based on the distance between the selected pixel and the data-line drive circuit (22), a boosted, high voltage is supplied to the data line X in a given period within the selection period)**.*

Regarding claim 15, Morita teaches a driving circuit *(Fig. 9 (12, 20, 22, 25, 26))* for a liquid crystal display *(col. 10, lines 62-64, LCD device, see Fig. 9)* which comprises a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells *(col. 7, lines 20-43, Fig. 9 (10, M(m, n), Y, X, 30), pixels formed in the*

liquid crystal panel 10 are defined by M(1, 1) to M(m, n), where m and n are

natural numbers, a liquid crystal panel 10 has (m.times.n) pixels (e.g.,

m=800 and n=600 in the embodiment), for one pixel M(1, 1), a data line

X.sub.1 is connected to the source of a thin film transistor (TFT) device 30

and a line Y.sub.1 is connected to the gate thereof, data lines X.sub.1 to

X.sub.m are driven by a data-line drive circuit 22 and the voltage

transformation circuit 25, while lines Y.sub.1 to Y.sub.n are driven by the

line drive circuit 20), the driving circuit comprising means for successively generating a

plurality of write-in voltages of a line signal of a video frame at end points of said column

lines*(col. 3, lines 59-60, Fig. 9 (22), a data line drive circuit (22) which*

supplies a data signal to each of the data lines, col. 7, lines 54-56, the

signal control section 12 sends data signals Da, a clock signal CLK1 and a

horizontal sync signal Hsync to the data-line drive circuit 22, col. 8, lines 5-

6, the data signal voltage vd is output from the data-line drive circuit 22,

note that as shown in Fig. 9, data lines X.sub.1 to X.sub.m are driven by a

data-line drive circuit 22), successively selecting each of said row lines *(col. 2, lines 4-*

6, Fig. 9 (20), a scan-line drive circuit (20) which supplies a scan signal to

each of the scan lines for selecting one of the scan lines); and supplying said

write-in voltages from said end points of the column lines to the liquid crystal cells of the

selected row line for a period corresponding to a geometric distance from the selected row line to

said end points*(col. 12, lines 51-59, Fig. 9 (22, 24), the data signal voltage to*

be supplied to the individual pixels corresponding to the line that is to be

*scanned is changed by the **voltage transformation circuit (24). Based***

on the distance between the selected pixel and the data-line drive

circuit (22), a boosted, high voltage is supplied to the data line X in

***a given period within the selection period**).*

Regarding claims 2 and 16, Morita teaches said driving circuit *(Fig. 9 (12, 20, 22,*

25, 26)) comprising a buffer memory *(Fig. 9 (12))* for storing said video frame *(col. 11,*

lines 3-5, col. 7, line 54, as shown in Fig. 9, a signal control section 12 sends

data signals Da, a clock signal CLK1, a horizontal sync signal Hsync, and

vertical sync signal Hsync, note that as shown in Fig. 9, those signals are

acquired externally, and in order to process and send those signals, it is

inherent that the control section (12) possess memory); a timing controller *(col.*

Fig. 9 (12)) for generating first and second timing signals *(col. 7, lines 54-56, col. 7,*

lines 66-67, signal control section 12 sends a clock signal, CLK1 to the data-

line drive circuit 22, a clock signal, CLK2 to the line drive circuit 20, note

that it is inherent that the control section (12) generates those CLK signals

before it sends them); a column driver *(Fig. 9 (22))* for receiving a line signal from said

memory *(Fig. 9 (12))*, converting said line signal to said write-in voltages and supplying said

write-in voltages to said column lines in response to said first timing signal *(col. 7, lines 54-*

65, the data-line drive circuit 22 receives data signals Da, a clock signal

CLK1 and a horizontal sync signal Hsync from the signal control section (12).

The data-line drive circuit 22 latches the data signals Da, **at the timing of**

the clock signal CLK1, and based on the horizontal sync signal Hsync, the

latched one line of data signals Da is converted to analog signals which are

then subjected to impedance conversion. Each resultant signal is supplied to

the data line X as a data signal voltage Vd); and a row driver (Fig. 9 (20)) for

successively selecting each of said row lines for an interval between successive ones of said

second timing signal and supplying said write-in voltages to the liquid crystal cells of the

selected row line for a write-in period which runs from said first timing signal to said second

timing signal (col. 8, lines 1-7, the line drive circuit 20 sequentially switches a

line Y to be selected **at the timing of the clock signal CLK2**. In a period

where a specific line Y is selected, a voltage V.sub.2 to enable the gate of

the TFT device 30 connected to that line Y is applied. In synchronism with

the enabling of the gate, the data signal voltage vd output from the data-line

drive circuit 22 is supplied to the data line X, col. 7, lines 56-59, note that

the voltage Vd is the result of latched data signals Da at a timing of the clock

signal CLK1), said timing controller (Fig. 9 (12), control section (12) with timing

of CLK1, and timing of CLK2) generating said first timing signal at intervals increasingly

variable as a function of the geometric distance from the selected row line to said column driver

and generating said second timing signal at said increasingly variable intervals (col. 12, lines

39-43, as shown in FIG. 9, the voltage transformation circuit 25 sequentially

boosts the data signal voltages Vd to be supplied to the individual pixels

every time a single line is selected, col. 12, lines 55-59, note that a boosted,

high voltage is supplied to the data line X in a given period within the

selection period (T) based on the distance between the selected pixel and

the data-line drive circuit (22), col. 7, lines 56-59, note that the voltage Vd

is the result of latched data signals Da at a timing of the clock signal CLK1,

and col. 8, lines 1-2, the drive circuit 20 sequentially switches a line Y to be

selected at the timing of the clock signal CLK2).

Regarding claims 3 and 17, Morita teaches said write-in period is increasingly variable

from a nominal value *(Fig. 11(A-C) (t.sub.b1)) (col. 12, lines 18-20, as shown in*

Fig. 11B, a period from t.sub.1 is increasing, In Fig. 11 (B), the period from

t.sub.1 to t.sub.b3 is set shorter than the corresponding period from t.sub.1

to t.sub.b1 in FIG. 10B. Likewise, in FIG. 11C, a period from t.sub.1 to

t.sub.c3 is set shorter than the corresponding period from t.sub.1 to t.sub.c1

in FIG. 10C.)

Regarding claim 12, Morita teaches step (a) comprises the step of buffering a line signal

in a memory *(col. 3, lines 59-60, Fig. 9 (22) a data line drive circuit (22) which*

supplies a data signal to each of the data lines, col. 7, lines 54-56, note that

the signal control section 12 sends data signals Da, a clock signal CLK1 and

a horizontal sync signal Hsync to the data-line drive circuit 22, note that as

shown in Fig. 9, those signals are acquired externally, and in order to

process and send those signals, it is inherent that the control section (12)

possess memory) (c) and wherein step comprises the step of increasingly varying said

write-in period from a nominal value *(Fig. 11B (t.sub.1))* as a function of said distance

(col. 12, lines 18-19, **as shown in Fig. 11B, the data signal voltage, Vd**

is boosted in a period from t.sub.1 to t.sub.b3, *col. 12, lines 55-57,*

note that a boosted voltage is supplied to the data line X in a given period

within a selection period based on the distance between the selected pixel

and the data line drive circuit).

Regarding claim 25, Morita teaches said plurality of write-in voltages are of a constant

applied voltage (col. 12, lines 51-59, Fig. 9 (22, 24), based on the distance between the selected

pixel and the data-line drive circuit (22), a boosted, high voltage is supplied to the data line X in

a given period within the selection period, note that it is inherent that the data line X constantly

applies voltage to pixels)

Regarding claim 26, Morita teaches said period corresponding to a distance increases as a

function of the distance from the selected row line to said end points (col. 12, lines 51-59, Fig. 9

(22, 24), based on the distance between the selected pixel and the data-line drive circuit (22), a

boosted, high voltage is supplied to the data line X in a given period within the selection period,

note that the distance between the data-line drive circuit (22) and each pixel is different

vertically).

Regarding claim 27, Morita teaches said period is a variable period that varies based on

the distance from the selected row line to said end points (col. 12, lines 51-59, Fig. 9 (22, 24),

based on the distance between the selected pixel and the data-line drive circuit (22), a boosted,

high voltage is supplied to the data line X in a given period within the selection period, note that

the distance between the data-line drive circuit (22) and each pixel is different vertically).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 5-6, 13 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Morita (USPN 6750840).

Regarding claims 5 and 19, Morita teaches said circuit *(Fig. 9 (12, 20, 22, 25,*

26)) comprises: a timing controller *(Fig. 9 (12))* for generating a first, second timing signals

and third timing signals *(col. 7, lines 54-56, col. 7, lines 66-67, signal control*

section 12 sends a clock signal, CLK1 to the data-line drive circuit 22, a clock

signal, CLK2 to the line drive circuit 20, note that it is apparent that the control section (12) generates those CLK signals before it sends them, as shown in Fig. 11B, there are three time periods, t.sub.1, t.sub.3 and t.sub.b4); a column driver *(Fig. 9 (22))* for converting a line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to the first timing signal *(col. 7, lines 54-65, the data-line drive circuit 22 receives data signals Da, a clock signal CLK1 and a horizontal sync signal Hsync from the signal control section (12). The data-line drive circuit 22 latches the data signals Da, **at the timing of the clock signal CLK1**, and based on the horizontal sync signal Hsync, the latched one line of data signals Da is converted to analog signals which are then subjected to impedance conversion. Each resultant signal is supplied to the data line X as a data signal voltage Vd.)*; a row driver *(Fig. 9 (20))* for successively selecting one of said row lines for an interval between successive ones of said second timing signal and supplying said write-in voltages to the liquid crystal cells of the selected row line *(col. 8, lines 1-7, the line drive circuit 20 sequentially switches a line Y to be selected **at the timing of the clock signal CLK2**. In a period where a specific line Y is selected, a voltage V.sub.2 to enable the gate of the TFT device 30 connected to that line Y is applied. In synchronism with the enabling of the gate, the data signal voltage vd output from the data-line drive circuit 22 is supplied to the data line X).*

Morita teaches the timing of the clock signal CLK1 (col. 7, line 58) and the timing of the clock signal CLK2 (col. 8, line 2). Note from Fig. 11B, an interval is constant up until time, t.sub.1, then an interval varies up until time t.sub.b4, and then pass time, t.sub.b4, an interval becomes constant again.

Morita also teaches as illustrated in FIGS. 10A to 10C and FIGS. 11A to 11C, it is possible to execute such control as to charge each pixel selected in the predetermined period t by boosting the predetermined voltage V.sub.1 to a certain voltage level and changing the period in which the boosted voltage is applied (col. 12, lines 26-30). Note that a boosted voltage is supplied to the data line X in a given period within a selection period based on the distance between the selected pixel and the data line drive circuit (col. 12, lines 55-57).

Morita does not specifically teach said timing controller generating each of said first and second timing signals at constant intervals and generating said third timing signal at intervals increasingly variable as a function of the distance from the selected row line to said column

driver.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize changeable period in which the boosted voltage is applied as illustrated in Fig.11B (by changing a portion of a period starting from t.sub.1 but before t.sub.b3 so as to extend the constant interval beyond t.sub.1) for the purpose of improving a charge characteristics of pixels as taught by Morita (col. 12, lines 26-27, col. 11, lines 48-51).

Morita teaches the drive circuit 20 sequentially switches a line Y to be selected at the timing of the clock signal CLK2 with an application of enabling voltage V.sub.2 (col. 8, lines 1-2).

Morita also teaches as illustrated in FIGS. 10A to 10C and FIGS. 11A to 11C, it is possible to execute such control as to charge each pixel selected in the predetermined period t by boosting the predetermined voltage V.sub.1 to a certain voltage level and **changing the period in which the boosted voltage is applied** (col. 12, lines 26-30).

Morita does not specifically teach a row driver supplying said write-in voltages for a

write-in period which runs from said first timing signal to said third timing signal.

It would have been obvious to one of ordinary skill in the art at the

time the invention was made to recognize changing the period in which the

boosted voltage is applied as illustrated in Fig.11B (by changing a portion of

a period starting from t.sub.1 but before t.sub.b3 so as to extend the

constant interval beyond t.sub.1) for the purpose of improving a charge

characteristics of pixels as taught by Morita (col. 12, lines 26-27, col. 11,

lines 48-51).

Regarding claims 6 and 20, Morita teaches said writing period is variable from a less-

than-nominal value to a nominal value *(Fig. 11B (t.sub.1)) (col. 12, lines 18-22, as*

shown in Fig. 11B, the data signal voltage, Vd is boosted from T.sub.1 to

t.sub.b3, note that by changing a portion of a period starting from t.sub.1

shown in Fig. 11B until the period reaches 2t.sub.1, the range can be

reached, note that a claim limitation, "a nominal value" corresponds to

t.sub.1 in Fig. 11B).

Regarding claim 13, Morita also teaches as illustrated in FIGS. 10A to 10C and FIGS. 11A to 11C, it is possible to execute such control as to charge each pixel selected in the predetermined period t by boosting the predetermined voltage V.sub.1 to a certain voltage level and changing the period in which the boosted voltage is applied (col. 12, lines 26-30). For example, Morita teaches as shown in Fig. 11B, the data signal voltage, Vd is boosted from period t.sub.1 to t.sub.b3, which is set shorter than the corresponding period from t.sub.1 to t.sub.b1 in FIG. 10B (col. 12, lines 18-20).

Morita does not teach step (c) of increasingly varying said write-in period as a function of said distance in a range from a less-than-nominal value to a nominal value.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize changeable period in which the boosted voltage is applied as illustrated in Fig.11B (by changing a portion of a period starting from time, t.sub.1 until the period reaches time, 2t.sub.1) for the purpose of improving a charge characteristics of pixels as taught by Morita (col. 12, lines 26-27, col. 11, lines 48-51).

Note that a claim limitation, "a nominal value" corresponds to t.sub.1 in Fig. 11B.

Allowable Subject Matter

6.   Claims 4, 7-10, 14, 18, and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685.

The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas I Abdulselam
Examiner
Art Unit 2629
October 6, 2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
2600